## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Hajime YAMAMOTO, et al.

Serial Number: Not Yet Assigned

Filed: August 26, 2003

For: METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE, AND METHOD

OF FORMING RESIST PATTERN

## **INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

August 26, 2003

Sir:

In compliance with 37 CFR 1.56, Applicants call to the attention of the Patent and Trademark

Office the reference listed on the attached PTO-1449.

A copy of the reference is enclosed herewith.

In the event there are any fees due in connection with the filing of this paper, please charge

Deposit Account No. 01-2340.

Respectfully submitted,

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DWH/jaz Atty. Docket No. **031029** Suite 1000 1725 K Street, N.W. Washington, D.C. 20006 (202) 659-2930

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PATENT TRADEMARK OFFICE

Enclosures: PTO-1449; References (1)

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INFORMATION DISCLOSURE STATEMENT PTO-1449			Atty. Docket No. 031029			Serial No. New Application		
			Applicant(s): Hajime YAMAMOTO, et al.					
			Filing Date: August 26, 2003			Group Art Unit: Not Yet Assigned		
U.S. PATENT DOCUMENTS								
Examiner Initial		Docume	ent No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
	AA							
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			F	OREIGN PA	TENT DOCUM	ENTS		
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	AF AG	T	nent No.	Date	Country	Transla (Yes or	No)	
	AF AG AH	T	nent No.	Date 03/17/98	Country	Transla (Yes or Yes-Ab	No)	
	AF AG AH	T	nent No.	Date 03/17/98	Country Japan	Transla (Yes or Yes-Ab	No)	

Date Considered

Examiner